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### **IEEE Transactions on Very Large Scale Integration (VLSI)**

Large-scale Incremental Processing Using Distributed Transactions and Notiï•cations Daniel Peng and Frank Dabek dpeng@google.com, fdabek@google.com Google, Inc. Abstract Updating an index of the web as documents are crawled requires continuously transforming a large repository of existing documents as new documents ar-rive.

## **Large-scale Incremental Processing Using Distributed**

Design and realization of microelectronic systems using VLSI/ULSI technologies requires close collaboration among scientists and engineers in the fields of systems architecture, logic and circuit design, chips and wafer fabrication, packaging, testing, and systems applications. Generation of specifications, design, and verification must be performed at all abstraction levels, including the ...

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IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS 1 A Word Line Pulse Circuit Technique for Reliable Magnetoelectric Random Access Memory Hochul Lee, Albert Lee, Shaodi Wang, Farbod Ebrahimi, Puneet Gupta, Pedram Khalili Amiri, Member, IEEE, and Kang L. Wang, Fellow, IEEE Abstract—A word line pulse (WLP) circuit scheme is pro-

## **IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI)**

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## **Transactions on Large-Scale Data- and Knowledge-Centered**

288 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 12, NO. 3, MARCH 2004 The Effect of LUT and Cluster Size on Deep-Submicron FPGA Performance and Density Elias Ahmed and Jonathan Rose Abstract—In this paper, we revisit the field-programmable gate-array (FPGA) architectural issue of the effect of logic block func-

## **288 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION**

Synergy between grids, P2P systems, and agent technologies is the key to data- and knowledge-centered systems in large-scale environments. This, the 33rd issue of Transactions on Large-Scale Data- and Knowledge-Centered Systems, contains five revised selected regular papers.

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## **Transactions on Large-Scale Data- and Knowledge-Centered**

3046 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 25, NO. 11, NOVEMBER 2017 TABLE I DESCRIPTION OF NOTATIONS USED IN OUR DISCUSSION stacked-domain design to that of a conventional design.2 By definition (see Table I), in a stacked-domain design, we

## **IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI)**

Transactions on Large-Scale Data and Knowledge-Centered Systems by Venkatesh J N, Uday Kiran Rage, P Krishna Reddy, Masaru Kitsuregawa in Transactions on Large-Scale Data and Knowledge-Centered Systems Report No: IIIT/TR/2018/-1 Centre for Data Engineering International Institute of Information Technology Hyderabad - 500 032, INDIA May 2018

## **Transactions on Large-Scale Data and Knowledge-Centered**

278 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 13, NO. 2, FEBRUARY 2005 A Transaction-Based Unified Architecture for Simulation and Emulation Soha Hassoun,

Senior Member, IEEE, Murali Kudlugi, Duaine Pryor, and Charles Selvidge Abstractâ€”The availability of millions of transistors on a single

### **278 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION**

12 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 20, NO. 1, JANUARY 2012 Fig. 4. Component library. (a) The MATLAB GUI presents the user with all of the available component libraries. (b) Expansion of the Analog Signal Processing

### **10 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI**

1412 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 18, NO. 10, OCTOBER 2010 Improving Multi-Level NAND Flash Memory ... We have the overall PDF as shown in the following: (2) where is the mean of the threshold voltage (i.e., the center of the distribution as shown in Fig. 2), and the constant can be solved based on .

### **1412 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION**

250 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 26, NO. 2, FEBRUARY 2018 The primary enabling components that realize fine grain adaptation with high efficiency are the voltage regulators (VRs) and power delivery system of the proposed platform. A suitable power delivery system based on available state-

### **IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI**

IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 26, NO. 1, JANUARY 2018 63 ... This requires a very large number of sample ... instead of sampling, using the natural probability density function (PDF)  $f(x)$ , one would sample a distorted PDF  $p(x)$  that biases the sampling to the important region, typically toward the tails ...

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210 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 16, NO. 2, FEBRUARY 2008 Exact Distribution of the Max/Min of Two Gaussian Random Variables Saralees Nadarajah and Samuel Kotz ... probability density functions of the max/min and an illustration of the re-

### **Exact Distribution of the Max/Min of Two Gaussian**

IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 25, NO. 1, JANUARY 2017 3 Bevan M. Baas (SMâ€™11) received the B.S. degree in electronic engineering from California Polytechnic State University, San Luis Obispo, CA, USA, in 1987, and the M.S. and Ph.D.

### **IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI**

IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS 1 Robust Design-for-Security Architecture for Enabling Trust in IC Manufacturing and Test Ujjwal Guin , Member, IEEE, Ziqi Zhou, Student Member, IEEE, and Adit Singh, Fellow, IEEE Abstractâ€”Due to the prohibitive costs of semiconductor man-

### **IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI**

IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. XX, NO. XX,

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Community/Investor Guidelines for Large-Scale Land Transactions July 2015 Republic of Ghana Ministry of Food and Agriculture. ... PDF Project Development Facility ... processes for large-scale investments have often excluded many community stakeholders, such as women, youth, and migrants. ...

### **Community/Investor Guidelines for Large-Scale Land**

2940 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 25, NO. 10, OCTOBER 2017 fabrication, the netlist is mapped and fabricated, but the layouts and fabricated chips are untrusted. Note that there exist other untrusted sources, like third-party intellectual property cores.

### **IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI)**

Emerging Hardware Trends in Large-Scale Transaction Processing MAY/JUNE 2015 69 less than three years away. Memory-oriented DBMSs will still be the best-performing system architecture for this hierarchy, because they don't use legacy architectural components from the 1970s designed to mask the latency of slow disks.<sup>7</sup>

### **Emerging Hardware Trends in Large-Scale Transaction Processing**

IEEE TRANSACTIONS ON NEURAL NETWORKS, VOL. 14, NO. 6, NOVEMBER 2003 1569 Simple Model of Spiking Neurons Eugene M. Izhikevich Abstract " A model is presented that reproduces spiking and bursting behavior of known types of cortical neurons. The model combines the bi- ... simulation of large-scale brain models. As we develop such large-scale

### **Simple Model of Spiking Neurons - Izhikevich**

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IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 25, NO. 7, JULY 2017 2109 Design Methodologies for Low-Power 3-D ICs With Advanced Tier Partitioning Moongon Jung, Member, IEEE, Taigon Song, Student Member, IEEE, Yarui Peng, Student Member, IEEE, and Sung Kyu Lim, Senior Member, IEEE

### **IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI)**

IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 13, NO. 2, FEBRUARY 2005 1 Energy Aware Wireless Systems with Adaptive Power-Fidelity Tradeoffs Vijay Raghunathan, Student Member, IEEE, Cristiano L. Pereira, Mani B. Srivastava, Senior Member, IEEE, and Rajesh K. Gupta, Fellow, IEEE

### **IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI)**

2626 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 25, NO. 9, SEPTEMBER 2017 1) Based on the detailed analysis on memory failure characteristics, we propose a novel priority-based SRAM sizing methodology to enhance SRAM fault tolerance ability. Different from previous sizing approaches, our

### **IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION - NDSU**

478 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 16, NO. 4, APRIL 2008 is therefore ideal for a real-time DRM system considering dynamic stress conditions. B. EM EM is a failure mechanism caused by the movement of metal atoms through wires, creating voids (vacancies) and hillocks

### **476 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION**

IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 20, NO. 9, SEPTEMBER 2012 1645 Compact Degradation Sensors for Monitoring NBTI and Oxide Degradation Prashant Singh, Eric Karl, Member, IEEE, David Blaauw, and Dennis Sylvester, Fellow, IEEE Abstractâ€”We designed two compact in situ NBTI and oxide

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IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS 1 DScanPUF: A Delay-Based Physical Unclonable Function Built Into Scan Chain Yu Zheng, Student Member, IEEE, Fengchao Zhang, Student Member, IEEE, and Swarup Bhunia, Senior Member, IEEE Abstractâ€”Physical unclonable function (PUF) has emerged

### **IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI**

IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 12, NO. 2, FEBRUARY 2004 185 Level Conversion for Dual-Supply Systems Fujio Ishihara, Farhana Sheikh, Member, IEEE, and Borivoje Nikolic, Member, IEEE Abstractâ€”Dual-supply voltage design using a clustered voltage scaling (CVS) scheme is an effective approach to reduce chip

### **IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION - People**

IEEE TRANSACTIONS ON PATTERN ANALYSIS AND MACHINE INTELLIGENCE, 2014 1 Human3.6M: ... large scale statistical models and detailed evaluation baselines for the dataset illustrating its diversity and the scope for improvement by future work in the research community. Our experiments show that our best large scale model can leverage our full ...

### **IEEE TRANSACTIONS ON PATTERN ANALYSIS AND MACHINE**

IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 20, NO. 1, JANUARY 2012 1 A MITE-Based Translinear FPAA Craig R. Schlottmann, Student Member, IEEE, David Abramson, and Paul E. Hasler, Senior Member, IEEE Abstractâ€”While the development of reconïƒigurable analog platforms is a blossoming ïƒield, the tradeoff between usability and

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3392 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 25, NO. 12, DECEMBER 2017 detecting malicious signals in the third-party IP cores [4], [11]. However, these tools suffer from the state space explosion problem, and hence cannot be used for verifying large designs individually. Some efforts have been made to combine theorem

### **3390 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION**

IEEE TRANSACTIONS ON PATTERN ANALYSIS AND MACHINE INTELLIGENCE (ACCEPTED, 2018) 1 Large-Scale Low-Rank Matrix Learning with Nonconvex Regularizers Quanming Yao, Member IEEE, James T. Kwok, Fellow IEEE, Taifeng Wang, Member IEEE, and Tie-Yan Liu, Fellow IEEE

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2 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS Fig. 2. Memory interface eye diagram for voltage and noise budgets. along with SPICE analysis, including detailed signal integrity and power integrity analyses; this can take months for a new design [4]. CACTI-IO is not a substitute for detailed analyses,

### **IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI**

654 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 26, NO. 4, APRIL 2018 Fig. 1. (a) Integer-N PLL block diagram (key nonidealities that cause reference spurs are highlighted).

**IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI)**

IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 23, NO. 2, FEBRUARY 2015 317 Scan Test of Die Logic in 3-D ICs Using TSV Probing Brandon Noia, Shreepad Panth, Krishnendu Chakrabarty, Fellow, IEEE, and Sung Kyu Lim Abstract—Prebond testing of through-silicon-vias (TSVs) and

**IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI)**

IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 13, NO. 7, JULY 2005 819 Global Passivity Enforcement Algorithm for Macromodels of Interconnect Subnetworks Characterized by Tabulated Data Dharmendra Saraswat, Student Member, IEEE, Ramachandra Achar, Senior Member, IEEE, and Michel S. Nakhla, Fellow, IEEE

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